Partial English Translation of

LAID OPEN unexamined

JAPANESE PATENT APPLICATION

Publication No. 11-40804

[0014] to [0034]

[0014]

[Embodiments]

<First Embodiment> Figure 1 illustrates a semiconductor device fabrication method according to the first embodiment of the present invention. A polysilicon gate pattern is formed on a Si substrate (1) of which active region is defined by a LOCOS oxide film (2) and has a p-well region (3) formed by doping B. More specifically, a gate oxide film (4) having a thickness of 10 nm is formed on the active region, a polysilicon film (5) having a thickness of 250 nm and having p doped therein is formed thereon, and a Si_3N_4 film (6) having a thickness of 50 nm is formed by chemical vapor growth (hereinafter referred to as thermal CVD method), using thermal reaction. Further, the Si_3N_4 film (6) and the polysilicon film (5) are processed into the gate electrode pattern by a photoetching step. Furthermore, As ions are implanted to form a LDD (lightly doped drain) region (7) (Figure 1(a)).

[0015] A SiO_2 film (8) is formed to 100 nm on the Si substrate by the thermal CVD method (Figure 1(b)).

[0016] A part of the SiO_2 film (8) other than a side spacer (9) is removed by anisotropic dry etching (Figure 1(c)). In this time, a shoulder part (10) of the polysilicon gate pattern may be exposed to a degree, as shown in the drawing.

[0017] A thermal oxide film (11) having a thickness of 5 nm is formed on the LDD region (7). Simultaneously with this formation, a thermal oxide

film (12) is formed on the region where polysilicon is exposed, at the shoulder part (10) of the polysilicon gate pattern. However, the part of the gate electrode pattern other than the shoulder part (10) is covered with the Si_3N_4 film (6), thereby not being oxidized. The function of the thermal oxide film (11) is only to suppress reaction between a Co film formed thereon in the following step and the Si substrate therebelow. Hence, as long as the reliability can be guaranteed, the thinner the film (11) is, the more desirable it is, and more concretely, 2 nm or more is sufficient for the thermal oxide film (11) to exhibit this function. In the present embodiment, the film thickness thereof is set 5 nm (Figure 1(d)).

[0018] As ions are implanted into a source/drain region (13) and a dopant where the ions have been implanted is activated by rapid heating for 10 seconds at a temperature of 900 ℃. Further, the Si_3N_4 film (6) on the polysilicon layer (5) of the gate electrode is removed with heated phosphoric acid. The thermal oxide film (11) and the thermal oxide film (12) are not etched in this removal step, and accordingly, Si is exposed only on the polysilicon layer (5) (Figure 1(e)).

[0019] As conditions that the Si_3N_4 film (6), which is removed in this step, is required to satisfy, there are listed three conditions: The first is durability to etching the SiO_2 film (8) for the side spacer formation; The second is durability to the thermal oxide film (11) formation for preventing the polysilicon layer (5) below the Si_3N_4 film (6) from being oxidized. Lastly, the film (6) can be etched under such conditions that the thermal oxide film (11) is not etched. A silicon nitride film typified by the Si_3N_4 film formed by the thermal CVD method is suitable as a material which satisfies the above conditions.

[0020] By a DC magnetron sputtering method, a Co film (14) is formed to 10 nm on the entire surface of the substrate and a TiN film (15) is formed to 10 nm thereon (Figure 1(f)).

[0021] A cobalt silicide layer is selectively formed only on the gate

electrode where Co is in contact with Si by a thermal treatment under a nitrogen atmosphere at a temperature of 550 ℃ for 30 seconds. Herein, the cobalt silicide has a composition in which Co : Si is 1 : x ($x<1$). After the non-reacting Co film (14) and the non-reacting TiN film (15) are removed by wet etching, a thermal treatment is performed under a nitrogen atmosphere at a temperature of 750 ℃ for 30 seconds so that a cobalt silicide layer (16) is converted into a stoichiometic compound ($CoSi_2$) in which Co : Si is 1 : 2. Finally, the thickness of the cobalt silicide layer (16) is 45 nm (Figure 1(g)).

[0022] The thermal oxide film (11) on the surface of the Si substrate is removed with a mixture solution of a hydrofluoric acid solution and an ammonium fluoride solution. With the mixture solution of a hydrofluoric acid solution and an ammonium fluoride solution, it is possible to remove the thermal oxide film as a target while etching a negligible amount of the cobalt silicide layer (16). More specifically, when the mixture solution contains a hydrofluoric acid solution having a concentration of 50 % and an ammonium fluoride solution having a concentration of 40 % in a ratio of 1 : 20, the cobalt silicide ($CoSi_2$) film is etched at a rate of 2 nm or less per minute, which is one tenth or less of 30 nm per minute (a ratio at which the SiO_2 film is etched with this mixture solution). Although the etching is performed for 15 seconds for removing the thermal oxide film (11) having a thickness of 5 nm in the present embodiment, no difference in the thickness of the cobalt silicide ($CoSi_2$) film is admitted between before and after the etching (Figure 1(h)).

[0023] Thereafter, by the DC magnetron sputtering method, a Co film (17) is formed to 10 nm on the entire surface of the substrate and a TiN film (18) is formed to 10 nm thereon.

[0024] A cobalt silicide layer is selectively formed on the region of the Si substrate (1) where Si is exposed and on the gate electrode by a thermal treatment under a nitrogen atmosphere at a temperature of 550 ℃ for 30

seconds. Herein, the cobalt silicide has a composition in which Co : Si is 1 : x (x<1). After the non-reacting Co film (17) and the non-reacting TiN film (18) are removed by wet etching, a thermal treatment is performed under a nitrogen atmosphere at a temperature of 750 ℃ for 30 seconds so that a cobalt silicide layer (19) and a cobalt silicide layer (20) are each converted into a stoichiometic ratio compound ($CoSi_2$) in which Co : Si is 1 : 2. The cobalt silicide layer has a thickness of 80 nm in a region on the gate electrode where silicide is formed twice and has a thickness of 45 nm in a region where silicide is formed once (Figure 1(j)).

[0025] It is to be noted that the p-MOS transistor can be formed in the same manner as the n-MOS transistor formation method explained in the present embodiment. Further, in a case where the p-type polysilicon is used for the gate electrode of the p-MOS transistor and the p-MOS transistor and the n-MOS transistor are separately formed for the dual gate, an implantation mask is formed in the photoresist step after the gate polysilicon layer is formed and B and P are separately implanted into the p-type polysilicon region and the n-type polysilicon region, respectively.

[0026] <Second Embodiment> Figure 2 illustrates a semiconductor device fabrication method according to the second embodiment of the present invention. A polysilicon gate pattern is formed on a Si substrate (21) of which An active region is defined by a LOCOS oxide film (22) and has a p-well region (23) formed by doping B. More specifically, a gate oxide film (24) having a thickness of 10 nm is formed on the active region, and a polysilicon film (25) having a thickness of 250 nm is formed thereon and is processed into the gate electrode pattern by a photoetching step. Furthermore, As ions are implanted to form a LDD region (26) (Figure 2(a)).

[0027] A Si_3N_4 film (27) having a thickness of 30 nm is formed on the entire surface of the Si substrate by the thermal CVD method, and a SiO_2 film (28) having a thickness of 70 nm is formed thereon also by the

thermal CVD method (Figure 2(b)).

[0028] After the SiO_2 film (28) is etched by an anisotropic etching technique, a part of the SiO_2 film (28) other than a side spacer (29) is removed and etching is halted at the Si_3N_4 film (27) therebelow. Although the Si_3N_4 film is hardly etched under the conditions for etching the SiO_2 film, a shoulder part (30) of the polysilicon gate pattern is cut by the components of spatters at etching, thereby being exposed, as shown in the drawing. The etching amount at the shoulder part (30) is adjustable according to the etching time period. In the present embodiment, etching is performed until a region (31) which is left at the center of the gate has a width of 150 nm with regard to a gate width 250 nm (Figure 2(c)).

[0029] As ions are implanted onto the Si substrate through the Si_3N_4 film (27) so that a source/drain region (32) is formed, and a dopant of ions implanted therein is activated by a short-time thermal treatment at a temperature of 900 ℃ for 10 seconds (Figure 2(d)).

[0030] By the DC magnetron sputtering method, a Co film (33) having a thickness of 10 nm is formed on the entire surface of the substrate and a TiN film (34) having a thickness of 10 nm is formed thereon (Figure 2(e)).

[0031] A cobalt silicide layer (35) is selectively formed only at the shoulder part of the gate pattern where Co is in contact with Si, in a manner that a thermal treatment is performed under a nitrogen atmosphere at a temperature of 550 ℃ for 30 seconds. In this time, the cobalt silicide has a composition in which Co : Si is 1 : x ($x<1$). After a non-reacting Co film and a non-reacting TiN film are removed by wet etching, a thermal treatment is performed under a nitrogen atmosphere at a temperature of 750 ℃ for 30 seconds so that the cobalt silicide layer (35) is converted into a stoichiometic compound ($CoSi_2$) in which Co : Si is 1 : 2. Finally, the thickness of the cobalt silicide layer (35) is 45 nm (Figure 2(f)).

[0032] A Si_3N_4 film in the region (31) on the gate polysilicon layer is

removed with heated phosphoric acid. Cobalt silicide is hardly etched under the conditions for etching Si_3N_4 (Figure 2(g)).

[0033] By the DC magnetron sputtering method, a Co film (36) having a thickness of 10 nm is formed on the entire surface of the substrate and a TiN film (37) having a thickness of 10 nm is formed thereon (Figure 2(h)).

[0034] A cobalt silicide layer (38) and a cobalt silicide layer (39) are selectively formed only on the exposed surface of Si and the gate electrode by a thermal treatment is performed under a nitrogen atmosphere at a temperature of 550 ℃ for 30 seconds. Herein, the cobalt silicide has a composition in which Co : Si is 1 : x ($x<1$). After the non-reacting Co film (17) and the non-reacting TiN film (18) are removed by wet etching, a thermal treatment is performed under a nitrogen atmosphere at a temperature of 750 ℃ for 30 seconds so that a cobalt silicide layer (38) and a cobalt silicide layer (39) are each converted into a stoichiometic compound ($CoSi_2$) in which Co : Si is 1 : 2. The cobalt silicide layers have a thickness of 80 nm in a region on the gate electrode where silicide is formed twice and a thickness of 45 nm in a region where silicide is formed once, respectively (Figure 2(i)).